IN THE SPECIFICATION:

The paragraph beginning on page 2 line 17 is amended as follows:

These and other objective are achieved in the present invention by providing an integrated circuit with an on-chip jitter measurement circuit. The on-chip jitter measurement circuit comprises a plurality of delay elements, a first set of circuitry and a second set of circuitry. The delay elements each have an associated delay, an input configured to receive an input clock signal and an output responsive to the associated delay and [[the]] input clock signal. The input clock signal has a significant instant. The first set of circuitry is connected to the inputs and outputs of the plurality of delay elements. Moreover, the first set of circuitry is also configured to detect the significant instant [[on]] of the input clock signal. The first set of circuitry is also configured to output a signal responsive to the significant instant [[on]] of the input clock signal. The second set of circuitry is configured to receive the signal responsive to the significant instant [[on]] of the input clock signal and a first trigger signal. Also, the second set of circuitry is configured to latch onto the signal responsive to the significant instant [[on]] of the input clock signal and is further responsive to a significant instant [[on]] of the first trigger signal. A measure for jitter is determined from the latched signal responsive to the significant instant [[on]] of the input clock signal.

The paragraph beginning on page 3 line 5 is amended as follows:

In another embodiment of the invention, the latched signal is filtered. In yet another embodiment, latched signal is recorded for a plurality of significant instants [[on]] of the first trigger signal. In another embodiment of the invention, a result calculator is configured to provide information collected from the measure of jitter.

The paragraph beginning on page 3 line 9 is amended as follows:

A method is also disclosed for measuring jitter of a significant instant [[on]] of an input clock signal derived from a reference clock signal. The method comprises the steps of receiving an input clock signal, delaying the input clock signal, receiving a trigger

signal and producing a jitter measurement signal. The input clock signal has a significant instant. The input the input clock signal is delayed by a first delay to produce a delayed clock signal and a delayed significant instant on the delayed input clock signal. The trigger signal is delayed from the reference clock signal by a second delay. The jitter measurement signal is responsive to the delayed significant instant [[on]] of the delayed input clock signal and the trigger signal.

The paragraph beginning on page 4 line 13 is amended as follows::

Figure 1 is a timing diagram illustrating significant time instants [[on]] of a reference clock signal and an input signal according to an embodiment of the invention;

The paragraph beginning on page 4 line 28 is amended as follows:

Shown in Figure 1 is a reference clock signal 102 and input clock signals 104 and 106. Reference clock signal 102 can be, for example and without limitation, a master clock signal generated externally from a microprocessor or can be an internally generated clock signal within an application specific integrated circuit (ASIC). Moreover, reference clock signal 102 can be derived from another clock signal. Input clock signals 104 and 106 can be, for example and without limitation, clock signals received at an input to a microprocessor or communication circuit. Significant instants of reference clock signal 102 include rising edges 102-0 and 102-2 (note that various occurrences of similar events are indexed as "-x") and the falling edges 102-1. As shown input clock signals 104 and 106 have corresponding significant instants shown as rising edges 104-0 and 106-0, respectively. Also shown is dashed line 108 corresponding to an expected time E(t) 110 corresponding to the time when the rising edges of input clock signals 104 and 106 is expected to occur. Deviations from the expected time E(t) 110 are considered jitter. As shown, rising edge 104-0 of input clock signal 104 occurs earlier in time than expected time E(t) 110. The difference in time is measured as Δtl 112 and rising edge 104-0 is said to lead expected time E(t) 110. Moreover, rising edge 106-0 of input clock signal 106 occurs later in time than expected time E(t) 110. The difference in time is measured as Δt2 114 and [[on]] rising edge 106-0 is said to lag expected time E(t).

The paragraph beginning on page 5 line 24 is amended as follows:

With the understanding of jitter, a method of the present invention for measuring jitter can be understood as shown in the flowchart of [[Figures]] Figure 2A and the block diagram of Figure 2B. In receiving an input clock signal at step 250 of Figure 2A, the input clock signal is delayed at step 252 by a predetermined amount. This predetermined amount can be related to an expected amount of delay due to a clock signal propagating through circuits and sub-circuits. A trigger signal is provided as step 254 that is related to an instant in time when a significant instant [[on]]of the delayed input clock signal is expected to occur. Jitter measured as the[[measures a]] difference in time, Δt, between the occurrence of a significant time instant [[on]]of the delayed input clock signal and the trigger signal, is calculated at step 256. The calculated jitter result is then output at step 258.